AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A video data transfer method of a ~~liquid crystal~~ display device comprising:

converting ~~for transferring~~ input video data that is composed of parallel data ~~as~~ into partially serialized output video data;

determining whether ~~to a signal line driving circuit, said video data transfer method characterized in that, in the event that~~ the a bit inversion number between first data ~~positioned previously~~ and second data following said first data of said partially serialized output video data is more than half or not; and

~~positioned subsequently in a continuous sequence of said output video data is more than half of the bit number of the output video data, an inversion process for~~ inverting a logic state of said second data if the bit inversion number is more than half.~~the succeeding output video data is performed at a stage of said input video data that is composed of the parallel data~~.

2. (currently amended): A video data transfer method of a ~~liquid crystal~~ display device comprising:

~~for~~ serializing input video data of a 3 X 2^n-bit parallel in a 2^m-bit unit (n and m: natural numbers larger than zero, n > m) to produce ~~transfer it as~~ output video data of a 3 X $2^{(n-m)}$-bit parallel; and

controlling, ~~to a signal-line driving circuit, said video data transfer method characterized in that an inversion or a noninversion of~~every 3 X $2^{(n-m)}$ bits, a polarity of ~~a succeeding bit is made for each of 3 X $2^{(n-m)}$~~ bits of said input video data that corresponds to ~~3 X $2^{(n-m)}$ bit parallel data of~~ said output video data so that the bit inversion number between ~~previously~~ first data and second data following said first data of ~~positioned data and subsequently positioned data of a~~ the 3 X $2^{(n-m)}$-bit parallel ~~of said output video data~~ is 3 X $2^{(n-m-1)}$ or less.

3. (original): A display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data to a signal-line driving circuit, said display control circuit characterized in having:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with a noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on of the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit unit to output it as the output video data and an output inversion signal.

4. (currently amended): A display control circuit <u>comprising:</u>

~~for inputting input video data of a 3 X 2^n bit parallel to transfer it as output video data serialized in a 2^m bit (n and m: natural numbers, n > m) unit of a first bit, a second bit, ..., and a 2^m th bit to a signal line driving circuit, said display control circuit characterized in comprising:~~

~~—~~a first ~~comparison~~ comparator which is configured to compare ~~determination means for comparing~~ a noninversion bit of the 2^m-th bit of previous data having a 2^m-bit unit with the noninversion bit of the first bit of subsequent data having a 2^m-bit unit to determine whether ~~or not~~ the bit inversion number is more than half,

a second ~~comparison~~ comparator which is configured to compare ~~determination means for comparing~~ an inversion bit of the 2^m-th bit of the previous data having a 2^m-bit unit with the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit to determine whether ~~or not~~ the bit inversion number is more than half,

a third ~~comparison~~ comparator which is configured to compare ~~determination means for comparing~~ the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether ~~or not~~ the bit inversion number is more than half;

a fourth ~~comparison~~ comparator which is configured to compare ~~determination means for comparing~~ the inversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether ~~or not~~

~~the bit inversion number is more than half, ...,~~ 2 x 2^m-1-th comparators ~~comparison determination means~~ which are configured to compare ~~for comparing~~ the noninversion bit of the

2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether ~~or not~~ the bit inversion number is more than half,

2 x 2^m-th determining units which are configured to compare~~comparison determination means for comparing~~ the inversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether ~~or not~~ the bit inversion number is more than half;

a selector comprising a first selector, a second selector, ..., and a 2^mth selector, which are configured to select and output the output of either of the determination results of said first and second determining units, the output of either of the determination results of said third and fourth determining units, ..., and the output of either of the determination results of said 2 X 2^{m-1}th and said 2 X 2^mth comparators, respectively, said first selector ~~selection means that is composed of first selection means, second selection means, ..., and 2^m-th selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, the output of either of the determination results of said third comparison determination means and said fourth comparison determination means, ..., and the output of either of the determination results of said 2 x 2^m-1-th comparison determination means and said 2 x 2^m-th comparison determination means respectively, said first selection means~~ being controlled by the output of the 2^m-th ~~selection~~ selector ~~means~~ based on the input video data that is one piece of the data ahead, said second ~~selection means~~selector being controlled by the output of the first selector, ~~selection means,~~ ...,

said 2^m-th ~~selection~~ selector ~~means~~ being controlled by the output of the 2^m-1-th ~~selection means~~selector;

an output circuit, which is configured to ~~output means for~~, based on the outputs of said first ~~selection~~ selector~~means~~, said second ~~selection~~ selector~~means~~, ..., and said 2^m-th ~~selection~~ selector~~means~~ of said ~~selection~~ selectors~~means~~, ~~making~~ make an inversion or a noninversion of the first bit, the second bit, ..., and the 2^m-th bit of said subsequent data, respectively, and to output them along with ~~, and for outputting~~ an inversion signal indicating said inversion or noninversion; and

—a parallel-to-serial conversion circuit ~~for serializing~~which is configured to serialize the output of said output means in a 2^m-bit unit and to output ~~it~~ the serialized data as the output video data and an output inversion signal.

5. (original): A liquid crystal display device comprising: a display control circuit for inputting input video data that is composed of parallel data to transfer video data obtained by serializing each piece of the input video data in a two-bit unit of a first bit and a second bit as output video data; and a signal-line driving circuit for inputting said output video data, said liquid crystal display device characterized in that said display control circuit comprises:

first comparison determination means for comparing a noninversion bit of the second bit of previous data with the noninversion bit of the first bit of subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

second comparison determination means for comparing an inversion bit of the second bit of the previous data with the noninversion bit of the first bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data with the noninversion bit of the second bit of the subsequent data to output a determination result as to whether or not the bit inversion number is more than half;

selection means that is composed of first selection means and second selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, and the output of either of the determination results of said third comparison determination means and said fourth comparison determination means respectively, said first selection means being controlled by the output of the second selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means;

output means for, based on the output of said first selection means and the output of said second selection means of said selection means, making an inversion or a noninversion of the first bit of the subsequent data and the second bit of the subsequent data respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and

a parallel-to-serial conversion circuit for serializing the output of said output means in a two-bit unit to output it as the output video data and an output inversion signal.

6. (original): A liquid crystal display device comprising~~:~~ a display control circuit as claimed in claim 4.~~for inputting input video data of a 3 x 2^n-bit parallel to transfer video data serialized in a 2^m-bit (n and m: natural numbers, n > m) unit of a first bit, a second bit, …, and a 2^m-th bit as output video data; and a signal line driving circuit for inputting said output video data, said liquid crystal display device characterized in that said display control circuit comprisies:~~

~~— first comparison determination means for comparing a noninversion bit of the 2^m-th bit of previous data having a 2^m-bit unit with the noninversion bit of the first bit of subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, second comparison determination means for comparing an inversion bit of the 2^m-th bit of the previous data having a 2^m-bit unit with the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, third comparison determination means for comparing the noninversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, fourth comparison determination means for comparing the inversion bit of the first bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the second bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half,~~

~~...,2 x 2^m-1-th comparison determination means for comparing the noninversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half, 2 x 2^m-th comparison determination means for comparing the inversion bit of the 2^m-1-th bit of the subsequent data having a 2^m-bit unit with the noninversion bit of the 2^m-th bit of the subsequent data having a 2^m-bit unit to determine whether or not the bit inversion number is more than half;~~

~~— selection means that is composed of first selection means, second selection means, ..., and 2^m-th selection means for selecting/outputting the output of either of the determination results of said first comparison determination means and said second comparison determination means, the output of either of the determination results of said third comparison determination means and said fourth comparison determination means, ..., and the output of either of the determination results of said 2 x 2^m-1-th comparison determination means and said 2 x 2^m-th comparison determination means respectively, said first selection means being controlled by the output of the 2^m-th selection means based on the input video data that is one piece of the data ahead, said second selection means being controlled by the output of the first selection means, ..., said 2^m-th selection means being controlled by the output of the 2^m-1-th selection means;~~

~~— output means for, based on the outputs of said first selection means, said second selection means, ..., and said 2^m-th selection means of said selection means, making an inversion or a noninversion of the first bit, the second bit, ..., and the 2^m-th bit of said subsequent data~~

~~respectively to output them, and for outputting an inversion signal indicating said inversion or noninversion; and~~

~~a parallel-to-serial conversion circuit for serializing the output of said output means in a 2^m bit unit to output it as the output video data and an output inversion signal.~~

7. (new): The video data transfer method as claimed in claims 1, wherein bits of said second data are inverted before said second data is partially serialized.

8. (new): A display control circuit comprising:

a first comparator which is configured to compare a noninversion bit of second bits of a first data with a noninversion bit of first bits of a second data following said first data to output a first determination result as to whether the bit inversion number is more than half;

a second comparator which is configured to compare an inversion bit of said second bits of said first data with the noninversion bit of said first bits of said second data to output a second determination result as to whether the bit inversion number is more than half;

a third comparator which is configured to compare the inversion bit of first bits of said second data with the noninversion bit of the second bits of said second data to output a third determination result as to whether the bit inversion number is more than half;

a fourth comparator which is configured to compare the inversion bit of said first bits of said second data with the noninversion bit of the second bits of said second data to output a fifth determination result as to whether the bit inversion number is more than half;

a first selector which is configured to selectively output one of said first and second determination results, said first selector being controlled by the output of a second selector;

a second selector which is configured to selectively output one of said third and fourth determination results, said second selector being controlled by the output of the first selector;

an output circuit which is configured to output an inversed signal or a non-inverted signal of the first bits of the second data based on the output of said first selector and an inversed signal or a non-inverted signal of the second bits of the second data based on the output of said second selector, and to output an inversion signal indicating the inversion or non-inversion; and

a parallel-to-serial conversion circuit which is configured to serialize the output of said output circuit in a two-bit unit to output it as the output video data and an output inversion signal.

9. (new): A liquid crystal display device comprising the display control circuit as claimed in claim 8.

10. (new): A video data transfer method of a display device, the method comprising:

comparing odd numbered bits of first video data with even numbered bits of said first video data to output an inversion determination signal if said even numbered bits of said first video data are to be inverted; and

comparing said even numbered bits of said first video data with odd numbered bits of a second video data following said first video data to output an inversion determination signal if said odd numbered bits of said second video data are to be inverted.

11. (new): A display control circuit comprising:

a delay circuit which is configured to delay first bits corresponding to one of the odd numbered bits and one of the even numbered bits of video data and to output the delayed first bits;

a first comparator which is configured to compare said delayed first bits and second bits corresponding to the other of said odd numbered bits and even numbered bits of the video data; and

a second comparator which is configured to compare said first bits which are not delayed by said delay circuit with said second bits.

12. (new): The display control circuit as claimed in claim 11, further comprising:

a first control circuit which controls a polarity of said second bits based on the output of said first comparator; and

a second control circuit which controls a polarity of said first bits which are not delayed by said delay circuit based on the output of said second comparator.

13. (new): The display control circuit as claimed in claim 12, further comprising:

a data parallel to serial converter which is configured to receive the outputs of said first and second control circuits and to convert parallel video data including said first and second bits to serial video data.

14. (new): The display control circuit as claimed in claim 13, further comprising:

a signal parallel to serial converter which is configured to receive the outputs of said first and second comparators and to convert a parallel output data of said first and second comparators to a serial polarity control signal.